THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte LAWRENCE E. CONNELL

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Appeal No. 97-4407
Application 08/441,560[1]

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ON BRIEF

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Before HAIRSTON, JERRY SMITH and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

[1] Application for patent filed May 15, 1995.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 7, all of the claims pending in the present application.

The invention relates to electronic testing of digital integrated circuits. Appellant discloses on page 5 of the specification that Figure 1 is a system block diagram illustrating a general configuration of an addressable serial test system in accordance with a preferred embodiment of the invention. Serial shift or serial access register 103 is used to serially transfer both address and data for both controlling and observing internal logic nodes of a digital system. A data stream containing address and data information is serially applied to scan input 104 and clocked into serial access register 103. Once register 103 is loaded, the address information is applied to address bus 101 and data information is applied to a global bi-directional data bus 100.

The address is used to specify which subset of a multiplicity of subsets of the internal logic nodes are to be

selected, while the data is used to program the state of those nodes selected. The nodes are constructed of various forms of storage elements including latches, flip-flops and other memory elements.

On page 6 of the specification, Appellant discloses that address decoding logic 107 is remotely located near a subset of internal nodes, subsystem block 2, to be selected. Subsystem block 2 depicts a subset of internal storage nodes, memory elements A through P, which can be loaded with program data applied to data bus 100. During normal system operation, storage elements A through P operate as simple D flip-flops with a D data input, a C clock input and a Q output. During a test mode of operation, storage elements A through P are loaded with the program data supplied from the serial access register 103 via global bi-directional data bus 100. Once the serial access register 103 is loaded with the address and program data, the control input 102 is then enabled and the address decoder output 111 is activated. Address decoder 107 decodes the address received on address bus 101. Address decoder output 111 is applied to load control input LD of storage elements A through P.

When activated, input LD will then cause the program data applied to test inputs TI through data bus 100 to be loaded in parallel into storage elements A through P. Appellant discloses that this feature advantageously provides increased flexibility in specifying input test stimulus for each subset of internal nodes that are selected by the address.

The independent claim 1 is reproduced as follows:

1. An addressable serial test system comprising:

a serial shift register having a clock input, a serial data input, and a plurality of parallel outputs, wherein a data stream is clocked into the serial shift register via a shift clock signal and reflected at the plurality of outputs;

an address decoder having a plurality of inputs connected to a portion of the plurality of outputs of the serial shift register, and an output for providing a selection signal dependent on the data stream reflected at the portion of the plurality of outputs of the serial shift register;

a system clock for generating a system clock signal;

a storage element having a clock input coupled to the system clock signal, a data input residing at a logical state, an output, a load input coupled to the selection signal provided by the address decoder, and a test data input coupled to another portion of the plurality of outputs of the serial shift register, wherein the output is alternately forced to another logical state by the selection signal dependent on the data stream present at the test data input, and forced to the logical state of the data input by the system clock.

The Examiner relies on the following reference:

Edwards et al. (Edwards) 5,271,019 Dec. 14, 1993

Claims 1 through 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Edwards.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 7 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d

1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellant argues on pages 3 and 4 of the brief that Edwards fails to teach or suggest a storage element having a selection signal input coupled to the load output of the address decoder and a test data input element coupled to another portion of the plurality of outputs of the serial shift register. Appellant points out that with the claimed structure any data can be forced into the storage element in a test mode, where in the Edwards system the storage element can only be forced to one fixed logical state.

We note that Appellant’s independent claims 1, 4 and 6, all recite the above structure as argued by Appellant. In particular, Appellant's claim 1 recites "a storage element having a clock input coupled to the system clock signal, a data input residing at a logical state [and] an output." We note that Edwards teaches a storage element as shown in Figures 1A and 3

having a clock input, a data input D and an output Q. However, Appellant's claim 1 further recites that the storage element comprises "a load input coupled to the selection signal provided by the address decoder, and a test data input coupled to another portion of the plurality of outputs of the serial shift register, wherein the output is alternately forced to another logical state by the selection signal dependent on the data stream present at the test data input, and forced to the logical state of the data input by the system clock."

In reviewing Edwards, we fail to find that Edwards teaches or suggests this claimed structure, a load input and a test data input different from the data input. In column 4, lines 5-16, Edwards teaches that scan latches of a system under test are divided into groups in which each group may be addressed. In column 4, lines 27-40, Edwards teaches when a group is addressed, the addressed group is connected to a group addressing and initializing circuit. The circuit simultaneously initializes all the latches of an address group to a predefined initial state. In column 7, lines 3-13, Edwards teaches the structure of the scan latch. In particular, Edwards teaches that each scan latch has a D input terminal for receiving data and a Q output terminal for outputting the stored data. Also, each scan

latch has a clock input, a SET and RST for respectively setting the state of its stored data to all logic "1" or resetting it to a logic "0" irrespective of the data on the D input terminal. However, Edwards fails to teach or suggest the storage element having an additional load input coupled to the selection signal provided by the address decoder and an additional test data input

coupled to another portion of the plurality of outputs of the serial shift register as claimed by Appellant.

We have not sustained the rejection of claims 1 through 7 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES

)
MICHAEL R. FLEMING)
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